Introducing the IBM z13 Server

Jim Elliott, Consulting Sales Specialist, IBM Systems
IBM z13 platform positioning

Platform Core Capabilities:

- The world’s premier transaction and data engine now enabled for the mobile generation
- The integrated transaction and analytics system for right-time insights at the point of impact
- The world’s most efficient and trusted cloud system that transforms the economics of IT
IBM z13 Specifications

- Machine type – 2964
  - 5 models – NE1, NC9, N96, N63, N30
  - Up to 141 customer configurable engines
- Sub-capacity Offerings for up to 30 CPs
- PU (Engine) Characterization
  - CP, IFL, ICF, zIIP, SAP, IFP (No zAAPs)
- SIMD instructions, SMT for IFL and zIIP
- On Demand Capabilities
  - CoD: CIU, CBU, On/Off CoD, CPE
- Memory – up to 10 TB
  - Up to 10 TB per LPAR (if no FICON Express8)
  - 96 GB Fixed HSA
- Channels
  - PCIe Gen3 16 GBps channel buses
  - Six LCSSs, up to 85 LPARs
  - 4 Subchannel Sets per LCSS
  - FICON Express16S or 8S (8 Carry forward)
  - OSA Express5S (4S carry forward)
  - HiperSockets – up to 32
  - Flash Express
  - zEnterprise Data Compression
  - RDMA over CE (RoCE) with SR-IOV Support
- Crypto Express5S
- Parallel Sysplex clustering, PCIe Coupling, and InfiniBand Coupling
- IBM zAware: z/OS and Linux on z Systems
- Operating Systems
  - z/OS, z/VM, z/VSE, z/TPF, Linux on z Systems
IBM z13 Availability Dates (1 of 2)

- **March 9, 2015**
  - Features and functions for the z13
  - z13 Models N30, N63, N96, NC9, and NE1
  - z196 air-cooled EC upgrades to z13 air-cooled
  - z196 air-cooled EC upgrades to z13 water-cooled
  - z196 water-cooled EC upgrades to z13 water-cooled
  - zEC12 air-cooled EC upgrades to z13 air-cooled
  - zEC12 air-cooled EC upgrades to z13 water-cooled
  - zEC12 water-cooled EC upgrades to z13 water-cooled
  - Field installed features and conversions on z13 that are delivered solely through a modification to the machine’s Licensed Internal Code (LIC)

- **March 13, 2015**
  - z/VM V6.3 exploitation support for Simultaneous multithreading (SMT)

- **April 14, 2015**
  - TKE 8.0 LIC (#0877) on zEC12 and zBC12
  - TKE Workstation (#0847) on zEC12 and zBC12
  - TKE Smart Card Reader (#0891) on zEC12 and zBC12
  - TKE additional smart cards (#0892) on zEC12 and zBC12
  - 4767 TKE Crypto Adapter (#0894) on zEC12 and zBC12
  - Fill and Drain Kit (#3380) for zEC12
  - Fill and Drain adapter kit (#3379) for zEC12
  - Universal Lift Tool/Ladder (#3105) for zEC12 and zBC12
  - Universal Lift Tool upgrade kit (#3103) for zEC12 and zBC12
IBM z13 Availability Dates (2 of 2)

- **June 26, 2015**
  - MES features for z13 Models N30, N63, N96, NC9, and NE1
  - z/VM V6.3 support for Multi-VSwitch Link Aggregation
  - Support for 256 Coupling CHPIDs
  - HMC STP Panel Enhancements: Initialize Time, Set Date and Time, Time Zone, View-Only Mode
  - Fibre Channel Protocol (FCP) channel configuration discovery and debug
  - Improved High Performance FICON for z Systems (zHPF) I/O Execution at Distance
  - IBM zAware support for Linux on z Systems

- **September 25, 2015**
  - FICON Dynamic Routing
  - Forward Error Correction (FEC) for FICON Express16S
  - Storage Area Network (SAN) Fabric I/O Priority
z13 Continues the CMOS Mainframe Heritage Begun in 1994

Uniprocessor Single Thread MIPS Improvements and GHz Increases

1. Capacity and performance ratios are based on measurements and projections using standard IBM benchmarks in a controlled environment. The actual throughput that any user will experience will vary depending on considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload.

2. Number of PU cores for customer use
z13 Full and Sub-Capacity CP Offerings

- Subcapacity CPs, up to 30, may be ordered on ANY z13 model, if 31 or more CPs are ordered all must be full 7xx capacity
- All CPs on a z13 CPC must be the same capacity
- All specialty engines are full capacity.
- zIIP to CP ratio – 2:1 and is the same for CPs of any capacity. No zAAPs available on z13
- Only 30 CPs can have granular capacity but other PU cores may be characterized as full capacity specialty engines
- For no CPs, the capacity setting is 400
- Total of 231 Capacity settings
- PVU for z13 is 120
z13 z/Architecture Extensions

- **Two-way Simultaneous Multithreading (SMT) operation**
  - Up to two active execution threads per core can dynamically share the caches, TLBs and execution resources of each IFL and zIIP core. SMT is designed to improve both core capacity and single thread performance significantly.
  - PR/SM online logical processors to dispatches physical cores; but, an operating system with SMT support can be configured to dispatch work to a thread on an IFL or zIIP core in single thread or SMT mode so that HiperDispatch cache optimization is considered. (Zero, one or two threads can be active in SMT mode). Enhanced hardware monitoring support will measure thread usage and capacity.

- **Core micro-architecture radically altered to increase parallelism**
  - New branch prediction and instruction fetch front end to support SMT and to improve branch prediction throughput.
  - Wider instruction decode, dispatch and completion bandwidth: Increased to six instructions per cycle compared to three on zEC12
  - Larger instruction issue bandwidth: Increased to up to 10 instructions issued per cycle (2 branch, 4 FXU, 2 LSU, 2 BFU/DFU/SIMD) compared to 7 on zEC12
  - Greater integer execution bandwidth: Four FXU execution units
  - Greater floating point execution bandwidth: Two BFUs and two DFUs; improved fixed point and floating point divide

- **Single Instruction Multiple Data (SIMD) instruction set and execution: Business Analytics Vector Processing**
  - Data types: Integer: byte to quad-word; String: 8, 16, 32 bit; binary floating point
  - New instructions (139) include string operations, vector integer and vector floating point operations: two 64-bit, four 32-bit, eight 16-bit and sixteen 8-bit operations.
  - Floating Point Instructions operate on newly architected vector registers (32 new 128-bit registers). Existing FPRs overlay these vector registers.
Simultaneous Multithreading (SMT)

- Simultaneous multithreading allows instructions from one or two threads to execute on a zIIP or IFL processor core.
- SMT helps to address memory latency, resulting in an overall capacity* (throughput) improvement per core.
- Capacity improvement is variable depending on workload. For AVERAGE workloads the estimated capacity* of a z13:
  - zIIP is 40% greater than a zEC12 zIIP
  - IFL is 32% greater than a zEC12 IFL
  - zIIP is 72% greater than a z196 zIIP
  - IFL is 65% greater than a z196 IFL
- Exploitation: z/VM V6.3+ for IFLs and z/OS V2.1+ for zIIPs
- SMT can be turned on or off on an LPAR by LPAR basis by operating system parameters. z/OS can also do this dynamically with operator commands.
  1. SMT is designed to deliver better overall capacity (throughput) for many workloads. Thread performance (instruction execution rate for an individual thread) may be faster running in single thread mode.
  2. Because SMT is not available for CPs, LSPR ratings do not include it.

* Capacity and performance ratios are based on measurements and projections using standard IBM benchmarks in a controlled environment. Actual throughput that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload.

** Two lanes at 50 carry 25% more volume if traffic density per lane is equal

Which approach is designed for the highest volume** of traffic?
Which road is faster?
SIMD (Single Instruction Multiple Data) processing

- Increased parallelism to enable analytics processing
  - Fewer instructions helps improve execution efficiency
  - Process elements in parallel enabling more iterations
  - Supports analytics, compression, cryptography, video/imaging processing

**Value**
- Enable new applications
- Offload CPU
- Simplify coding

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**Scalar**
Single Instruction, Single Data

```
A3 + B3 = C3
A2 + B2 = C2
A1 + B1 = C1
```

**SIMD**
Single Instruction, Multiple Data

```
{A3, A2, A1} + {B3, B2, B1} = {C3, C2, C1}
```

Instruction is performed for every data element

Perform instructions on every element at once
More memory makes a difference

- Up to 10 TB available memory
- Transparently support shrinking batch windows and meet service goals – no change to applications needed to gain benefits
- Get more work done – online transaction processing can experience up to 70% reduction in response time with more memory
- Improve system performance, minimize constraints and simplify management of applications with database middleware exploitation of additional memory
- Adding additional memory can increase sales and client satisfaction when you cut response time in half
- Achieve faster decision making with the advantages of in memory data
- Improves real to virtual ratio that allows deployment and support for more Linux workloads
z13 8-Core Processor Unit (PU) Chip Detail

- **14S0 22nm SOI Technology**
  - 17 layers of metal
  - 3.99 Billion Transistors
  - 13.7 miles of copper wire

- **Chip Area**
  - 678.8 mm²
  - 28.4 x 23.9 mm
  - 17,773 power pins
  - 1,603 signal I/Os

- **Up to eight active cores (PUs) per chip**
  - 5.0 GHz (vs. 5.5 GHz zEC12)
  - L1 cache/core
    - 96 KB I-cache
    - 128 KB D-cache
  - L2 cache/core
    - 2M+2M Byte eDRAM split private L2 cache

- **Single Instruction/Multiple Data (SIMD)**
- Single thread or 2-way simultaneous multithreading (SMT) operation

- **Improved instruction execution bandwidth:**
  - Greatly improved branch prediction and instruction fetch to support SMT
  - Instruction decode, dispatch, complete increased to 6 instructions per cycle
  - Issue up to 10 instructions per cycle
  - Integer and floating point execution units

- **On chip 64 MB eDRAM L3 Cache**
  - Shared by all cores

- **I/O buses**
  - One GX++ (InfiniBand) I/O bus
  - Two PCIe I/O buses

- **Memory Controller (MCU)**
  - Interface to controller on memory DIMMs
  - Supports RAIM design
z13 System Controller (SC) Chip Detail

- **CMOS 14S0 22nm SOI Technology**
  - 15 Layers of metal
  - 7.1 Billion transistors
  - 12.4 Miles of copper wire

- **Chip Area**
  - 28.4 x 23.9 mm
  - 678 mm²
  - 11,950 power pins
  - 1,707 Signal Connectors

- **eDRAM Shared L4 Cache**
  - 480 MB per SC chip (Non-inclusive)
  - 224 MB L3 NIC Directory
  - 2 SCs = 960 MB L4 per z13 drawer

- **Interconnects (L4 – L4)**
  - 3 to CPs in node
  - 1 to SC (node – node) in drawer
  - 3 to SC nodes in remote drawers

- **6 Clock domains**
z13 SCM vs. zEC12 MCM Comparison

z13 Single Chip Modules (SCMs)

- **Processor Unit (PU) SCM**
  - 68.5mm x 68.5mm – fully assembled
  - PU Chip area 678 mm²
  - Eight core chip with 6, 7 or 8 active cores

- **System Controller (SC) SCM**
  - 68.5mm x 68.5mm – fully assembled
  - SC Chip area 678 mm²
  - 480 MB on-inclusive L4 cache per SCM
  - Non-Data Integrated Coherent (NIC) Directory for L3

- **Processor Drawer – Two Nodes**
  - Six PU SCMs for 39 PUs (42 PUs in Model NE1)
  - Two SC SCMs (960 MB L4)
  - N30: One Drawer, N63: Two Drawers,
    N96: Three Drawers, NC9 or NE1: Four Drawers

zEC12 Multi Chip Module (MCM)

- **Technology**
  - 96mm x 96mm with 102 glass ceramic layers
  - 7,356 LGA connections to 8 chip sites

- **Six 6-core Processor (PU) chips**
  - Each with 4, 5 or 6 active cores
  - 27 active processors per MCM (30 in Model HA1)
  - PU Chip size 23.7 mm x 25.2 mm

- **Two System Controller (SC) chips per MCM**
  - 192 MB L4 cache per SC, 384 MB per MCM
  - SC Chip size 26.72 mm x 19.67 mm

- **One MCM per book, up to 4 books per System**
z13 Drawer Structure and Interconnect

Physical node: (Two per drawer)

- **Chips**
  - Three PU chips
  - One SC chip (480 MB L4 cache)

- **RAIM Memory**
  - Three Memory Controllers: One per CP Chip
  - Five DDR3 DIMM slots per Controller: 15 total per logical node
  - Populated DIMM slots: 20 or 25 per drawer

- **SC and CP Chip Interconnects**
  - X-bus: SC and CPs to each other (same node)
  - S-bus: SC to SC chip in the same drawer
  - A-bus: SC to SC chips in the remote drawers
Cache Topology – zEC12 vs. z13 Comparison

**zEC12 (Per Book)**

- **L1**: 64KI + 96KD
  6w DL1, 4w IL1
  256B line size

- **L2**: Private 1MB Inclusive of DL1
  Private 1MB Inclusive of IL1

- **L3**: Shared 48MB Inclusive of L2s
  12w Set Associative
  256B cache line size

- **L4**: 384MB Inclusive
  24w Set Associative
  256B cache line size

**z13 (half of CPC drawer node)**

- **L1**: 96KI + 128KD
  8w DL1, 6w IL1
  256B line size

- **L2**: Private 2MB Inclusive of DL1
  Private 2MB Inclusive of IL1

- **L3**: Shared 64MB Inclusive of L2s
  16w Set Associative
  256B cache line size

- **L4**: 480MB + 224MB NonData Inclusive Coherent Directory
  30W Set Associative
  256B cache line size
**z13 Processor Drawer (Top View)**

- **Two physical nodes, left and right**
- **Each logical node:**
  - One SC chip (480 MB L4 cache)
  - Three PU chips
  - Three Memory Controllers: One per CP Chip
  - Five DDR3 DIMM slots per Memory Controller: 15 total per logical node
- **Each drawer:**
  - Six PU Chips: 39 active PUs (42 in z13 Model NE1)
  - Two SC Chips (960 MB L4 cache)
  - Populated DIMM slots: 20 or 25 DIMMs to support up to 2,560 GB of addressable memory (3,200 GB RAIM)
  - Water cooling for PU and SC chips
  - Two Flexible Support Processors
  - Ten fanout slots for PCIe I/O drawer fanouts or PCIe coupling fanouts
  - Four fanout slots for IFB I/O drawer fanouts or PSIFB coupling link fanouts
z13 Radiator-based Air cooled – Front View (Model NC9 or NE1)

- Overhead Power Cables (option)
- Internal Batteries (optional)
- Power Supplies
- Displays and keyboards for Support Elements
- PCIe I/O drawers numbers 1 to 4 (Note: for an upgraded System, drawer slots 1 and 2 are used for the I/O Drawer)
- 2 x 1U Support Elements
- System Control Hubs (used to be BPHs)
- CPC Drawers, PCIe Fanouts, Cooling water manifold and pipes, PCIe I/O interconnect cables, FSPs and ethernet cables
- Note: CPC Drawer plugging numbers are on the left and logical numbers on the right
- Radiator Pumps
- Overhead I/O feature is a co-req for overhead power option

Note: for an upgraded System, drawer slots 1 and 2 are used for the I/O Drawer.
### z13 Processor Unit Allocation/Usage – zIIP to CP 2:1 ratio

<table>
<thead>
<tr>
<th>Model</th>
<th>Drawers/ PUs</th>
<th>CPs</th>
<th>IFLs ulIFLs</th>
<th>zIIPs</th>
<th>ICFs</th>
<th>Std SAPs</th>
<th>Optional SAPs</th>
<th>Std. Spares</th>
<th>IFP</th>
</tr>
</thead>
<tbody>
<tr>
<td>N30</td>
<td>1/39</td>
<td>0-30</td>
<td>0-30 0-29</td>
<td>0-20</td>
<td>0-30</td>
<td>6</td>
<td>0-4</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>N63</td>
<td>2/78</td>
<td>0-63</td>
<td>0-63 0-62</td>
<td>0-42</td>
<td>0-63</td>
<td>12</td>
<td>0-8</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>N96</td>
<td>3/117</td>
<td>0-96</td>
<td>0-96 0-95</td>
<td>0-64</td>
<td>0-96</td>
<td>18</td>
<td>0-12</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>NC9</td>
<td>4/156</td>
<td>0-129</td>
<td>0-129 0-128</td>
<td>0-86</td>
<td>0-129</td>
<td>24</td>
<td>0-16</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>NE1</td>
<td>4/168</td>
<td>0-141</td>
<td>0-141 0-140</td>
<td>0-94</td>
<td>0-141</td>
<td>24</td>
<td>0-16</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

- z13 Models N30 to NC9 use drawers with 39 cores. The Model NE1 has 4 drawers with 42 cores.
- The maximum number of logical ICFs or logical CPs supported in a CF logical partition is 16.
- The integrated firmware processor (IFP) is used for PCIe I/O support functions.
- Concurrent Drawer Add is available to upgrade in steps from model N30 to model NC9:
  1. At least one CP, IFL, or ICF must be purchased in every machine.
  2. Two zIIPs may be purchased for each CP purchased if PUs are available. This remains true for sub-capacity CPs and for “banked” CPs.
  3. On an upgrade from z196 or zEC12, installed zAAPs are converted to zIIPs by default. (Option: Convert to another engine type)
  4. “ulIFL” stands for Unassigned IFL.
  5. The IFP is conceptually an additional, special purpose SAP.
### z13 Purchased Memory Offering Ranges

<table>
<thead>
<tr>
<th>Model</th>
<th>Standard Memory GB</th>
<th>Flexible Memory GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>N30</td>
<td>64 - 2464</td>
<td>NA</td>
</tr>
<tr>
<td>N63</td>
<td>64 - 5024</td>
<td>64 - 2464</td>
</tr>
<tr>
<td>N96</td>
<td>64 - 7584</td>
<td>64 - 5024</td>
</tr>
<tr>
<td>NC9</td>
<td>64 - 10144</td>
<td>64 - 7584</td>
</tr>
<tr>
<td>NE1</td>
<td>64 - 10144</td>
<td>64 - 7584</td>
</tr>
</tbody>
</table>

- **Purchased Memory** – Memory available for assignment to LPARs
- **Hardware System Area** – Standard 96 GB of addressable memory for system use outside customer memory
- **Standard Memory** – Provides minimum physical memory required to hold customer purchase memory plus 96 GB HSA
- **Flexible Memory** – Provides additional physical memory needed to support activation base customer memory and HSA on a multiple CPC drawer z13 with one drawer out of service
- **Plan Ahead Memory** – Provides additional physical memory needed for a concurrent upgrade (LIC CC change only) to a preplanned target customer memory
### z13 Standard and Flexible Purchase Memory Offerings

<table>
<thead>
<tr>
<th>Memory Increment (GB)</th>
<th>Offered Memory Sizes (GB)</th>
<th>Memory Maximum Notes (GB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>64, 96, 128, 160,192</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>256, 320, 384, 448</td>
<td></td>
</tr>
<tr>
<td>96</td>
<td>544, 640, 736, 832, 928</td>
<td></td>
</tr>
<tr>
<td>128</td>
<td>1056, 1184, 1312, 1440</td>
<td></td>
</tr>
<tr>
<td>256</td>
<td>1696, 1952, 2208, <strong>2464</strong>, 2720, 2976, 3232, 3488, 3744, 4000, 4256, 4512, 4768, <strong>5024</strong>, 5280, 5536, 5792, 6048</td>
<td><strong>2464</strong> – N30 Standard, N63 Flexible</td>
</tr>
<tr>
<td>512</td>
<td>6560, 7072, <strong>7584</strong>, 8096, 8608, 9120, 9632, <strong>10144</strong></td>
<td><strong>7584</strong> – N96 Standard, NC9 and NE1 Flexible</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>10144</strong> – NC9 and NE1 Standard</td>
</tr>
</tbody>
</table>
IBM z13: Advanced system design optimized for digital business

System I/O Bandwidth
832 GB/Sec*

Memory
10 TB

MIPS for 1-way
1695

* No server can fully exploit its maximum I/O bandwidth
z Systems I/O Subsystem Internal Bus Interconnect

- **PCIe Gen3 z13**: 16 GBps
- **PCIe Gen2 z196/z114/z12**: 8 GBps
- **IFB z10/z196/z114/z12**: 6 GBps
- **STI z9**: 2.7 GBps
- **STI z990/z890**: 2 GBps
z13 “New Build” I/O and MES Features Supported

- **Features – PCIe I/O drawer**
  - FICON Express16S (SX and LX, 2 SFPs, 2 CHPIIDs)
  - FICON Express8S (SX and LX, 2 SFPs, 2 CHPIIDs)
  - OSA-Express5S
    - 10 GbE LR and SR (1 SFP, 1 CHPID)
    - GbE SX, LX, and 1000BASE-T (2 SFPs, 1 CHPID)
  - 10 GbE RoCE Express (2 supported SR ports)
  - zEDC Express
  - Crypto Express5S
  - Flash Express (technology refresh)

- **Integrated Coupling Adapter (ICA) Fanout**
  - PCIe-O SR two 8 GBps PCIe Gen3 Coupling Link

- **InfiniBand Coupling Feature Fanouts**
  - HCA3-O two 12x 6GBps InfiniBand DDR Coupling Links
  - HCA3-O LR four 1x 5Gbps InfiniBand DDR or SDR Coupling Links
z13 “Carry Forward” I/O Features Supported

- **Features – PCIe I/O drawer**
  - FICON Express8S (SX and LX, 2 SFPs, 2 CHPIDs)
  - OSA-Express5S (All)
  - OSA-Express4S (All)
  - 10 GbE RoCE Express (Both ports supported on z13)
  - zEDC Express
  - Flash Express
  - Not Supported: Crypto Express4S

- **Features – I/O drawer (No MES adds)**
  - FICON Express8 (SX and LX, 4 SFPs, 4 CHPIDs)
  - SoD: IBM plans to not support FICON Express8 on the next high-end z Systems server
  - Not Supported: ESCON, FICON Express4, OSA-Express3, ISC-3, and Crypto Express3

- **InfiniBand Coupling Features (Fanouts)**
  - HCA3-O two 12x 6GBps InfiniBand DDR Coupling Links
  - HCA3-O LR four 1x 5Gbps InfiniBand DDR or SDR Coupling Links
  - Not Supported: HCA2-O 12x, HCA2-O LR 1x InfiniBand Coupling Links
### z13 CPC Drawer and I/O Drawer Locations

- **Drawer locations are based on the front view of the machine:** Frame A (right), Frame Z (left) and EIA Unit location of the lower left of drawer corner
- **Locations are reported in eConfig “AO Data” reports along with PCHIDs for I/O definition
- **CPC Drawers are populated from bottom to top**
  - Drawer 1: A15A – N30, N63, N96, NC9 and NE1
  - Drawer 2: A19A – N63, N96, NC9 and NE1
  - Drawer 3: A23A – N96, NC9 and NE1
  - Drawer 4: A27A – NC9 and NE1
- **8-slot I/O drawers (if present) populate top down in Frame Z**
  - Drawer 1: Z22B, Drawer 2: Z15B: PCHID Range 100-17F
- **32-slot PCIe I/O Drawers populate in remaining locations:**
  - PCIe I/O Drawer 1: Z22B, Z15B or Z08B; PCHID Range 100-17F
  - PCIe I/O Drawer 2: Z15B, Z08B or Z01B; PCHID Range 180-1FF
  - PCIe I/O Drawer 3: Z08B, Z01B or A32A; PCHID Range 200-27F
  - PCIe I/O Drawer 4: Z01B; PCHID Range 280-2FF
  - PCIe I/O Drawer 5: A32A; PCHID Range 300-37F

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<table>
<thead>
<tr>
<th>FRAME</th>
<th>Z</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>42</td>
<td>IBF</td>
<td>SE Server</td>
</tr>
<tr>
<td>41</td>
<td>IBF</td>
<td>SE Server</td>
</tr>
<tr>
<td>40</td>
<td>IBF</td>
<td>IBF</td>
</tr>
<tr>
<td>39</td>
<td>BPA</td>
<td>I/O Drawer 5 Location A32A</td>
</tr>
<tr>
<td>38</td>
<td>SCH</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>I/O Drawer 1 Location Z22B</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>CPC Drawer 4 Location A27A</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>CPC Drawer 3 Location A23A</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>CPC Drawer 2 Location A19A</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>CPC Drawer 1 Location A15A</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>I/O Drawer 2 Location Z15B</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>I/O Drawer 3 Location Z08B</td>
<td>Radiator or Water Pumps</td>
</tr>
<tr>
<td>30</td>
<td>I/O Drawer 4 Location Z01B</td>
<td></td>
</tr>
</tbody>
</table>
Crypto Express5S Details

- **Native PCIe card (FC 0890)**
  - Resides in the PCIe I/O drawer
  - Requires CPACF Enablement (FC 3863)

- **New Crypto Module**
  - Designed to more than double Crypto Express4S performance (Added L2 Cache, New Crypto ASIC and processor upgrade)
  - Designed to support up to 85 domains for logical partitions or z/VM guests

- **Designed to Meet Physical Security Standards**
  - FIPS 140-2 level 4
  - ANSI 9.97
  - Payment Card Industry (PCI) HSM
  - Deutsche Kreditwirtschaft (DK)

- **New Functions, Standard and Compliance**
  - **Drivers:** NIST via FIPS standards and implementation guidance requirements; emerging banking standards: and strengthening of cryptographic standards for attack resistance
  - **VISA Format Preserving Encryption (VFPE)** for credit card numbers
  - Enhanced public key Elliptic Curve Cryptography (ECC) for users such a Chrome, Firefox, and Apple's iMessage

- **New Trusted Key Entry Workstation**
  - Workstation and LIC – FC 0847 with new crypto module and TKE LIC 8.0 is required
  - **Required:** EP11 (PKCS #11) Mode, **Recommended:** Common Cryptographic Architecture (CCA) Mode
  - Additional Smart Cards (FC 0892) – Support for stronger encryption than previous cards
FICON Express16S – SX and 10KM

- For FICON, zHPF, and FCP environments
  - CHPID types: FC and FCP
    - 2 PCHIDs/CHPIDs
- Auto-negotiates to 4, 8, or 16 Gbps
  - 2 Gbps connectivity not supported
  - FICON Express8S will be available to order for 2Gbps connectivity
- Increased bandwidth compared to FICON Express8S
- 10KM LX – 9 micron single mode fiber
  - Unrepeated distance – 10 kilometers (6.2 miles)
  - Receiving device must also be LX
- SX – 50 or 62.5 micron multimode fiber
  - Distance variable with link data rate and fiber type
  - Receiving device must also be SX
- 2 channels of LX or SX (no mix)
- Small form factor pluggable (SFP) optics
  - Concurrent repair/replace action for each SFP
**zHPF and FICON Performance** on z Systems

### I/O driver benchmark
- **IOs per second**
- **4k block size**
- **Channel 100% utilized**

<table>
<thead>
<tr>
<th>Channel</th>
<th>100% Utilized</th>
</tr>
</thead>
<tbody>
<tr>
<td>z10</td>
<td><strong>92000</strong></td>
</tr>
<tr>
<td>z10</td>
<td><strong>93000</strong></td>
</tr>
<tr>
<td>z10</td>
<td><strong>52000</strong></td>
</tr>
<tr>
<td>z10</td>
<td><strong>23000</strong></td>
</tr>
<tr>
<td><strong>14000</strong></td>
<td><strong>31000</strong></td>
</tr>
</tbody>
</table>

### Full-duplex
- **Large sequential read/write mix**

<table>
<thead>
<tr>
<th>Channel</th>
<th>100% Utilized</th>
</tr>
</thead>
<tbody>
<tr>
<td>z10</td>
<td><strong>2600</strong></td>
</tr>
<tr>
<td>z10</td>
<td><strong>1600</strong></td>
</tr>
<tr>
<td>z10</td>
<td><strong>770</strong></td>
</tr>
<tr>
<td>z10</td>
<td><strong>620</strong></td>
</tr>
<tr>
<td>z10</td>
<td><strong>520</strong></td>
</tr>
<tr>
<td><strong>350</strong></td>
<td><strong>520</strong></td>
</tr>
</tbody>
</table>

*This performance data was measured in a controlled environment running an I/O driver program under z/OS. The actual throughput or performance that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed.*

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FCP Performance* for z Systems

I/Os per second
Read/writes/mix
4k block size, channel 100% utilized

MegaBytes per second (full-duplex)
Large sequential
Read/write mix

*This performance data was measured in a controlled environment running an I/O driver program under z/OS. The actual throughput or performance that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed.
z/13 10GbE RoCE Express Feature

- Designed to support high performance system interconnect
  - Shared Memory Communication (SMC) over Remote Direct Memory Access (RDMA) (SMC-R) Architecture exploits RDMA over Converged Ethernet (CE) - RoCE
  - Shares memory between peers
  - Read/write access to the same memory buffers without application changes
  - Designed to increase transaction rates greatly with low latency and reduced CPU cost

- Configuration
  - z/13 – Both 10 GbE SFP+ ports enabled
  - z/13 – Support for up to 31 Logical Partitions
  - A switched connection requires an enterprise-class 10 GbE switch with SR Optics, Global Pause enabled and Priority Flow Control (PFC) disabled
  - Point-to-point connection is supported
  - Either connection supported to z/13, zEC12 and zBC12
  - Not defined as a CHPID and does not consume a CHPID number
  - Up to 16 features supported on a zBC12/zEC12
  - Link distance up to 300 meters over OM3 50 micron multimode fiber

- Exploitation and Compatibility
  - z/OS V2.1
  - z/VM V6.3 support for z/OS V2.1 guest exploitation
  - Linux on z Systems – IBM is working with Linux distribution partners to include support in future releases*

*Note: All statements regarding IBM’s plans, directions, and intent are subject to change or withdrawal without notice. Any reliance on these Statements of General Direction is at the relying party’s sole risk and will not create liability or obligation for IBM.
**z13 Parallel Sysplex Coupling Connectivity**

**z196 and z114**
12x IFB, 12x IFB3, 1x IFB

**zEC12 and zBC12**
12x IFB, 12x IFB3, 1x IFB

---

**IC (Internal Coupling Link):**
Only supports IC-to-IC connectivity

HCA2-O and HCA2-O LR are NOT supported on z13 or future High End z enterprises as Per SOD

ISC-3 is not supported on z13 even if I/O Drawer is Carried Forward for FICON Express8

Note: The link data rates in GBps or Gbps do not represent the performance of the links. The actual performance is dependent upon many factors including latency through the adapters, cable lengths, and the type of workload.

---

z10, z9 EC, z9 BC, z890, z990
Not supported in same Parallel Sysplex or STP CTN with z13
Performance Drivers with z13

- **Hardware**
  - Memory subsystem
    - Continued focus on keeping data "closer" to the processor unit
      - Larger L1, L2, L3, L4 caches
      - Improved IPC (Instructions Per Cycle)
    - 3x configurable memory
  - Processor
    - 2x instruction pipe width, re-optimized pipe depth for power/performance
      - Improved IPC
    - SMT for zIIPs and IFLs
      - Includes metering for capacity, utilization and adjusted chargeback (zIIPs)
    - SIMD unit for analytics
    - Up to 8 processor units per chip
    - Up to 141 configurable processor units
    - 4 different uni speeds

- **HiperDispatch**
  - Exploits new chip configuration
  - Required for SMT on zIIPs

- **PR/SM**
  - 85 customer partitions (up from 60)
  - Memory affinity
    - Keep LPARs, CPs, and memory local to drawer as much as possible
z13 vs. zEC12 Hardware Comparison

- **zEC12**
  - CPU
    - 5.5 GHz
    - Enhanced Out-Of-Order
  - Caches
    - L1 private 64k i, 96k d
    - L2 private 1 MB i + 1 MB d
    - L3 shared 48 MB / chip
    - L4 shared 384 MB / book

- **z13**
  - CPU
    - 5.0 GHz
    - Major pipeline enhancements
  - Caches
    - L1 private 96k i, 128k d
    - L2 private 2 MB i + 2 MB d
    - L3 shared 64 MB / chip
    - L4 shared 480 MB / node
z13 Capacity Performance Highlights

- Full speed capacity models ... capacity ratio to zEC12
  - Average 1.10x at equal n-way
  - Average 1.40x max capacity (141-way z13 vs. 101-way zEC12)

- Subcapacity models
  - Uniprocessor capacity ratio to full speed z13
    - 0.15x (target 250 MIPS)
    - 0.44x
    - 0.63x
  - Up to 30 CPs (general purpose processors) for each subcapacity model

- SMT capacity option
  - IFLs and zIIPs can optionally choose to run 2 hardware threads per processor engine or “core”
    - Opt-in or opt-out at the LPAR level
    - Added hardware threads appear as additional logical processors to z/VM and z/OS
  - May see wide range in capacity improvement per core over single thread: +10% to +40%

- Variability amongst workloads
  - Workloads moving to z13 can expect to see more variability than last migration
    - Performance driven by improved IPC in core and nest
      - Workloads will not react the same to the improvements in these areas
      - Micro benchmarks are particularly susceptible to this effect
SMT Performance Considerations

- SMT allows for the enablement of a second hardware thread per processor engine or “core”
  - Appears as another logical processor to z/VM and z/OS
  - LPARs may opt-in or opt-out to SMT on IFLs or zIIPs
- **Capacity gain per core will vary**
  - Dependent on the overlap and interference between the two threads
    - **Overlap**
      - Many core resources are replicated so each thread can make progress
      - While one thread waits for a cache miss, the other thread can continue to run
    - **Interference**
      - Some serialization points within the core
      - Threads share the same caches, thus cache misses can increase
  - Benchmarks observe +10% to +40% capacity increase versus single HW thread per core
    - No clear predictor of where a workload will fall
- **With SMT, individual tasks (SW threads) run slower but dispatcher delays reduce**
  - For example, a 1.3x capacity gain is spread over 2 hardware threads which means each thread runs at 1.3/2 = .65x a single thread or about the speed of a z196 core
  - But with twice as many hardware threads (logical processors) to dispatch to, dispatching delays (CPU queuing) can be reduced
- **Metering available through RMF and z/VM Performance Reports**
  - Thread density, utilization, capacity factors
Workload Variability with z13

- Performance variability is generally related to fast clock speed and physics
  - Increasing memory hierarchy latencies relative to micro-processor speed
  - Increasing sensitivity to frequency of "missing" each level of processor cache
  - Workload characteristics are determining factor, not application type

- z13 performance comes from improved IPC (instructions per cycle) in both the micro-processor and the memory subsystem (clock speed is 10% slower but tasks run on average 10% or more faster)
  - Magnitude of improvement in IPC will vary by workload
  - Workloads moving into a z13 will likely see more variation than last migration

- Use CPUMF to collect data for zPCR (and for IBM/BP to use with zCP3000)
Operating Systems focused on exploiting hardware innovation

**z/OS Version 2.1**
- Improved price performance for zIIP workloads with SMT
- Support new analytics workloads with SIMD
- New crypto capabilities for faster encryption
- Large memory to improve performance and enable new applications

**z/VM Version 6.3**
- Improved price performance with simultaneous multithreading technology – support for twice as many processors
- Improved systems management and economics
- Embracing Open Standards and Open Source Interoperability
- Supports more virtual servers than any other platform in a single footprint

**z/VSE Version 5.1**
- Reduced risk of access from unauthorized users
- Reduced memory constraints
- Wide portfolio using Linux on z
- Continued system usability enhancements with CICS Explorer
- More efficient communications

**Linux on z Systems**
- Multithreading allows for per core software savings
- Ability to host and manage more workloads efficiently and cost-effectively
- Automatic identification of unusual messages
- Integrated continuous availability & disaster recovery solution
## Operating System Support for z13

- Currency is key to operating system support and exploitation of future servers
- The following releases of operating systems will be supported on z13
  - Please refer to the PSP buckets for any required maintenance

<table>
<thead>
<tr>
<th>Operating System</th>
<th>Supported levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>z/OS</td>
<td>* z/OS V2.1 with PTFs (Exploitation)</td>
</tr>
<tr>
<td></td>
<td>* z/OS V1.13 with PTFs (Limited Exploitation)</td>
</tr>
<tr>
<td></td>
<td>* z/OS V1.12* with PTFs (End of service support 9/30/2014)</td>
</tr>
<tr>
<td>Linux on z Systems</td>
<td>* SUSE SLES 11 (Later releases: GA support TBD by SUSE.)</td>
</tr>
<tr>
<td></td>
<td>* Red Hat RHEL 6 and 7 (Later releases: GA support TBD by Red Hat.)</td>
</tr>
<tr>
<td>z/VM</td>
<td>* z/VM V6.3 with PTFs – Exploitation support</td>
</tr>
<tr>
<td></td>
<td>* z/VM V6.2 with PTFs – Compatibility plus Crypto Express5S support</td>
</tr>
<tr>
<td>z/VSE</td>
<td>* z/VSE V5.2 with PTFs – Compatibility plus Crypto Express5S (up to 85 LPARs)</td>
</tr>
<tr>
<td></td>
<td>* z/VSE V5.1 with PTFs – Compatibility</td>
</tr>
<tr>
<td>z/TPF</td>
<td>* z/TPF V1.1 – Compatibility</td>
</tr>
</tbody>
</table>

* *z/OS V1.12 will run on z13 provided the customer has IBM Software Support Services to get the PTFs*

* Beginning with z/OS V1.12, IBM Software Support Services replaces the IBM Lifecycle Extension for z/OS offering for extended support coverage for z/OS. The TSS Service Extension for z/OS is a fee-based Defect support (a fix, bypass, or restriction to a problem) for users who have not completed their migration to a newer z/OS release.

* Service extension support for z/OS V1.12 is provided for up to three years, beginning October 1, 2014 and available through September 30, 2017.

* Going forward, when support for a z/OS release is withdrawn, IBM Software Support Services intends to provide service extension support for the given z/OS release for up to three years. The intention is to provide an accommodation where additional time is needed to migrate to a newer z/OS release within the service support period. This does not alter the z/OS coexistence, migration, fallback, or service policy.
## z/OS Support Summary

<table>
<thead>
<tr>
<th>Release</th>
<th>z900/ z800 WdfM</th>
<th>z990/ z890 WdfM</th>
<th>z9 EC z9 BC WdfM</th>
<th>z10 EC z10 BC WdfM</th>
<th>z196 z114</th>
<th>zEC12 zBC12</th>
<th>zNext EC</th>
<th>End of Service</th>
<th>Extended Defect Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>z/OS V1.12</td>
<td>X</td>
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<td>9/14</td>
<td>9/17³*</td>
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<tr>
<td>z/OS V1.13</td>
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<td>X</td>
<td>9/16*</td>
<td>9/19³*</td>
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<tr>
<td>z/OS V2.1</td>
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<td>9/18*</td>
<td>9/21³*</td>
</tr>
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<td>X</td>
<td>X</td>
<td>X</td>
<td>9/20*</td>
<td>9/23³*</td>
</tr>
</tbody>
</table>

### Notes:

1. The IBM Lifecycle Extension for z/OS provides the ability for customers to purchase extended defect support for that release of z/OS for up to 24 months after the z/OS release’s end of service date.
2. Beginning with z/OS V1.12, IBM Software Support Services replaces the IBM Lifecycle Extension for z/OS offering with a service extension for extended defect support.

* Planned. All statements regarding IBM’s plans, directions, and intent are subject to change or withdrawal without notice.

WdfM  Server has been withdrawn from Marketing

### Legend

- Defect support provided with IBM Software Support Services for z/OS
- Generally supported
IBM z13 ITSO Publications

- **ITSO Redbooks/Redpapers**
  - New – IBM z13 Technical Introduction, SG24-8250
  - New – IBM z13 Configuration Setup, SG24-8260
  - Updated – IBM z Systems Connectivity Handbook, SG24-5444
  - Updated – IBM z Systems Functional Matrix, REDP-5157

- **ITSO Point-of-View Publicaions**
  - Securing your Mobile Mainframe, REDP-5176
  - z Systems Simultaneous Multithreading Revolution, REDP-5144
  - SIMD Business Analytics Acceleration on z Systems, REDP-5145
  - Enhancing Value to Existing and Future Workloads with IBM z13, REDP-5135
  - z/OS Infrastructure Optimization using Large Memory, REDP-5146
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